

FIG. 1

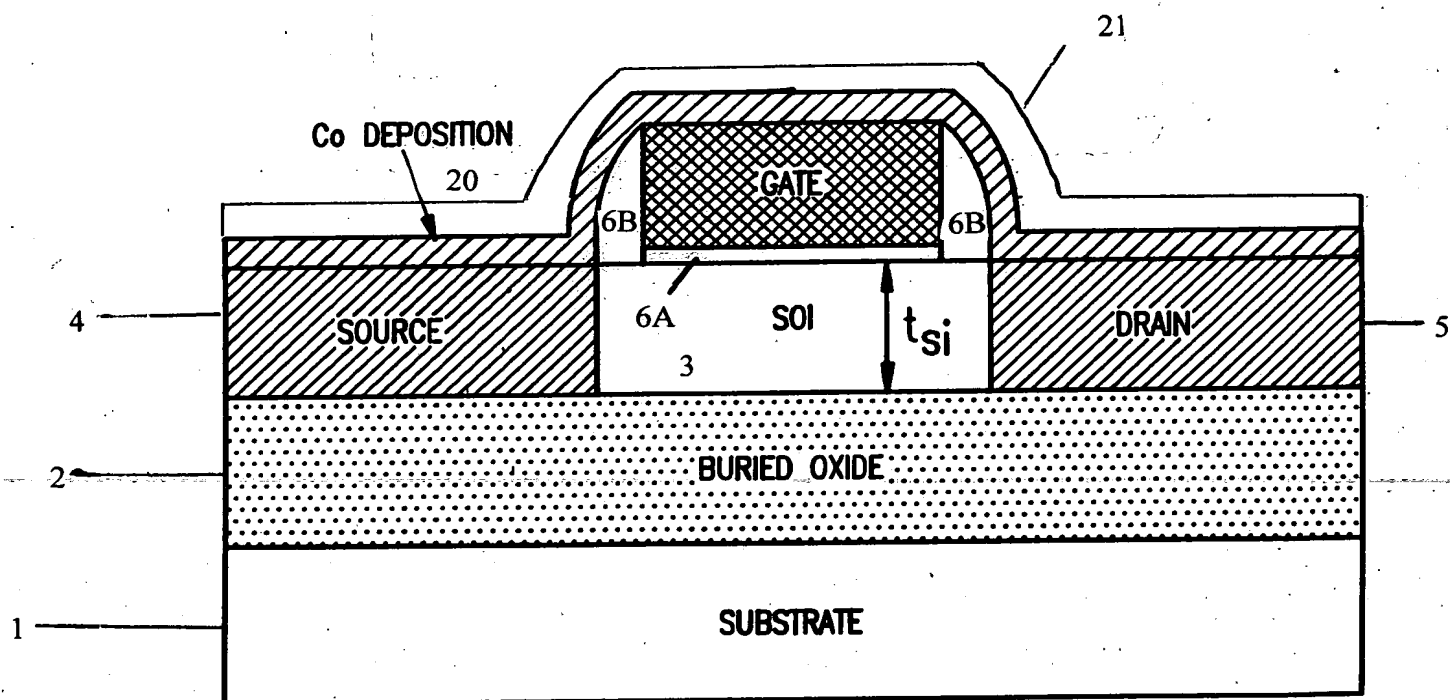


FIG. 2

A cross-sectional diagram of a Co₂Si gate SOI MOSFET structure. The diagram shows a substrate (1) at the bottom, followed by a buried oxide layer (2). Above the buried oxide is a silicon-on-insulator (SOI) layer (3) with thickness t_{si} . The SOI layer is divided into a central channel region (6A) and side regions (6B). A gate stack is formed on top of the channel region, consisting of a gate oxide layer (30) and a gate material layer (Co₂Si). The gate material layer is shown with a cross-hatched pattern. The side regions (6B) are also covered by a gate oxide layer (30) and a gate material layer (Co₂Si). The top surface of the gate material layer is labeled 'UNREACTED Co'. The source and drain regions are formed in the side regions (6B) and are labeled 'SOURCE' and 'DRAIN' respectively. The diagram is labeled with various numbers and text: 1, 2, 3, 5, 6A, 6B, 30, Co₂Si, UNREACTED Co, GATE, SOI, BURIED-OXIDE, SUBSTRATE, SOURCE, DRAIN, t_{si} .

DEPOSIT: a-Si

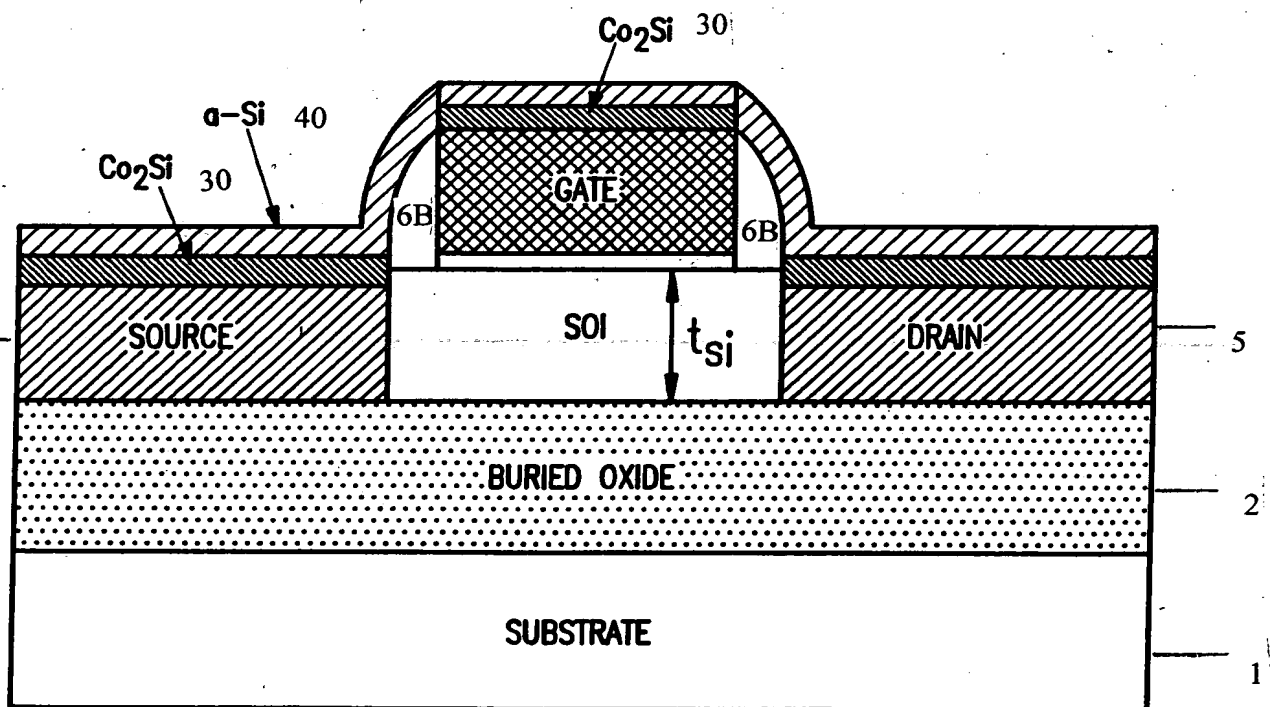


FIG.4

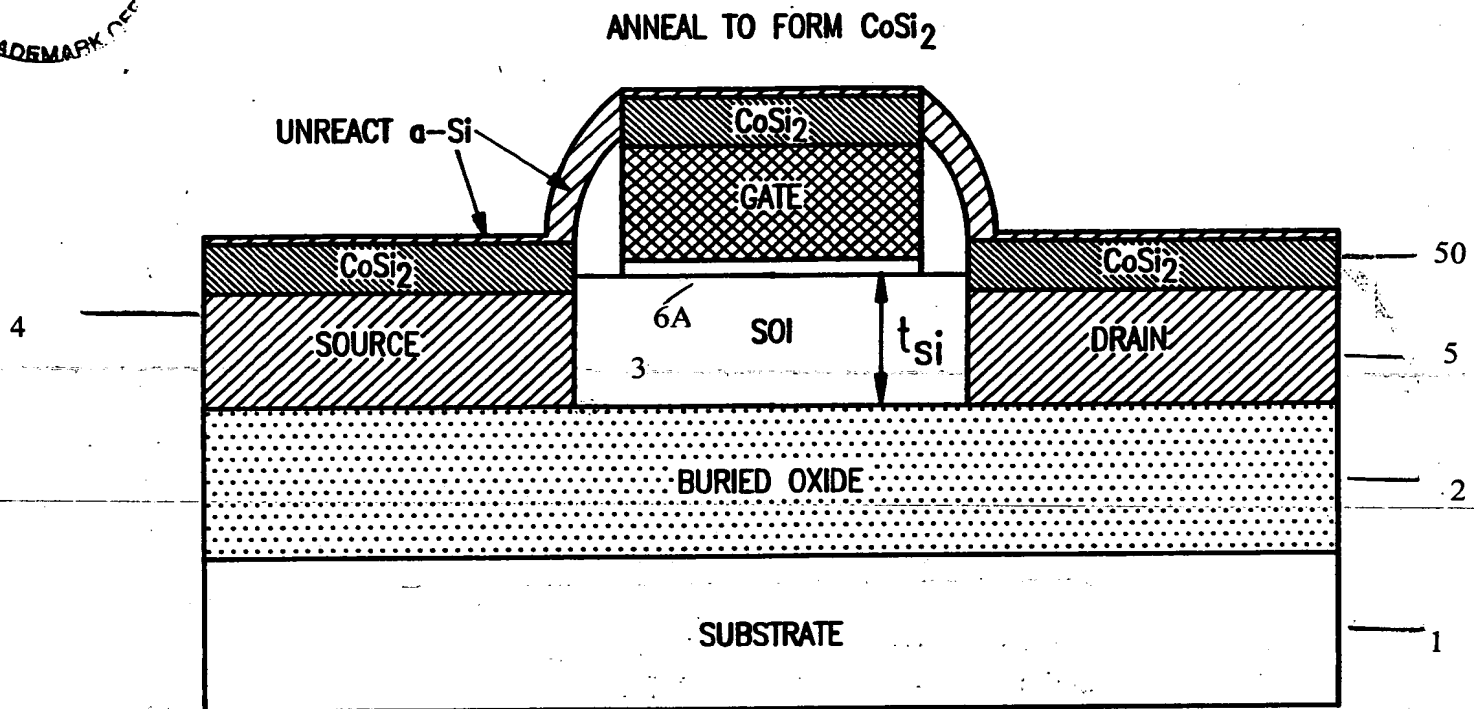


FIG.5

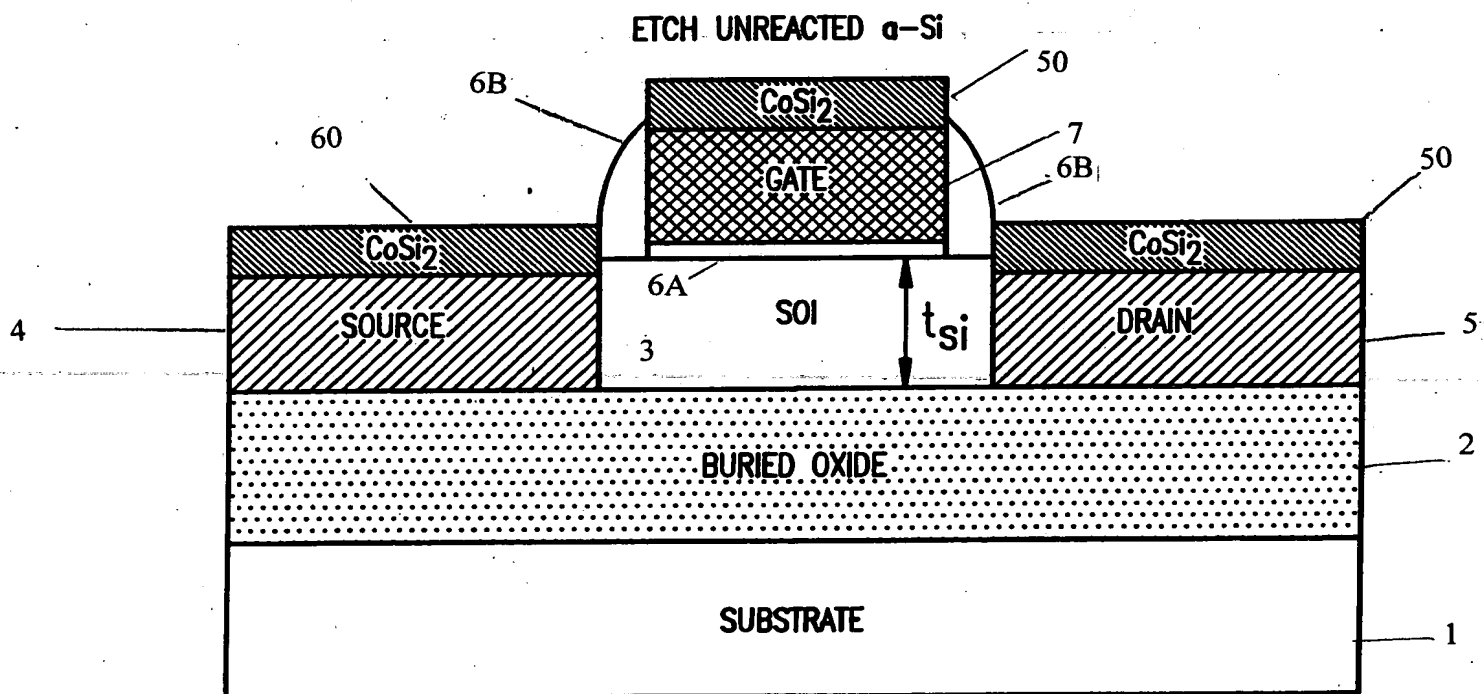


FIG.6

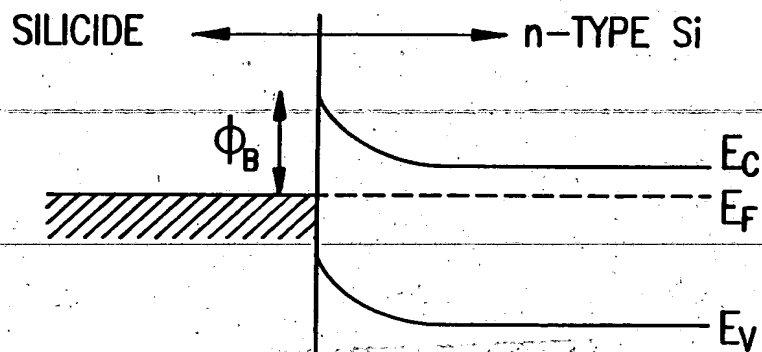


FIG. 7A

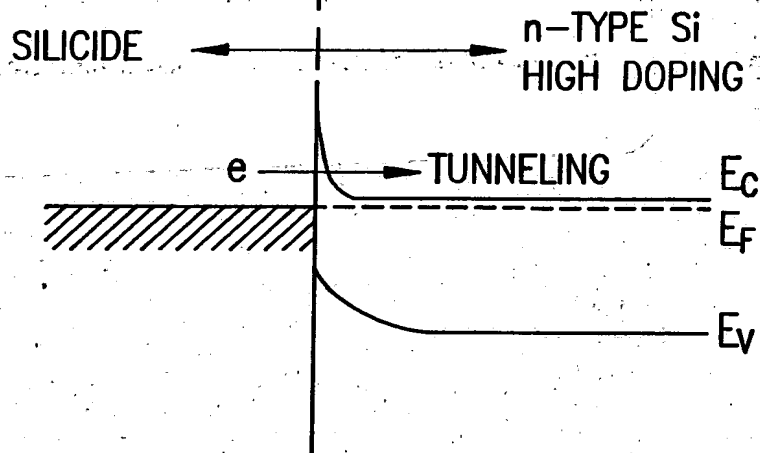
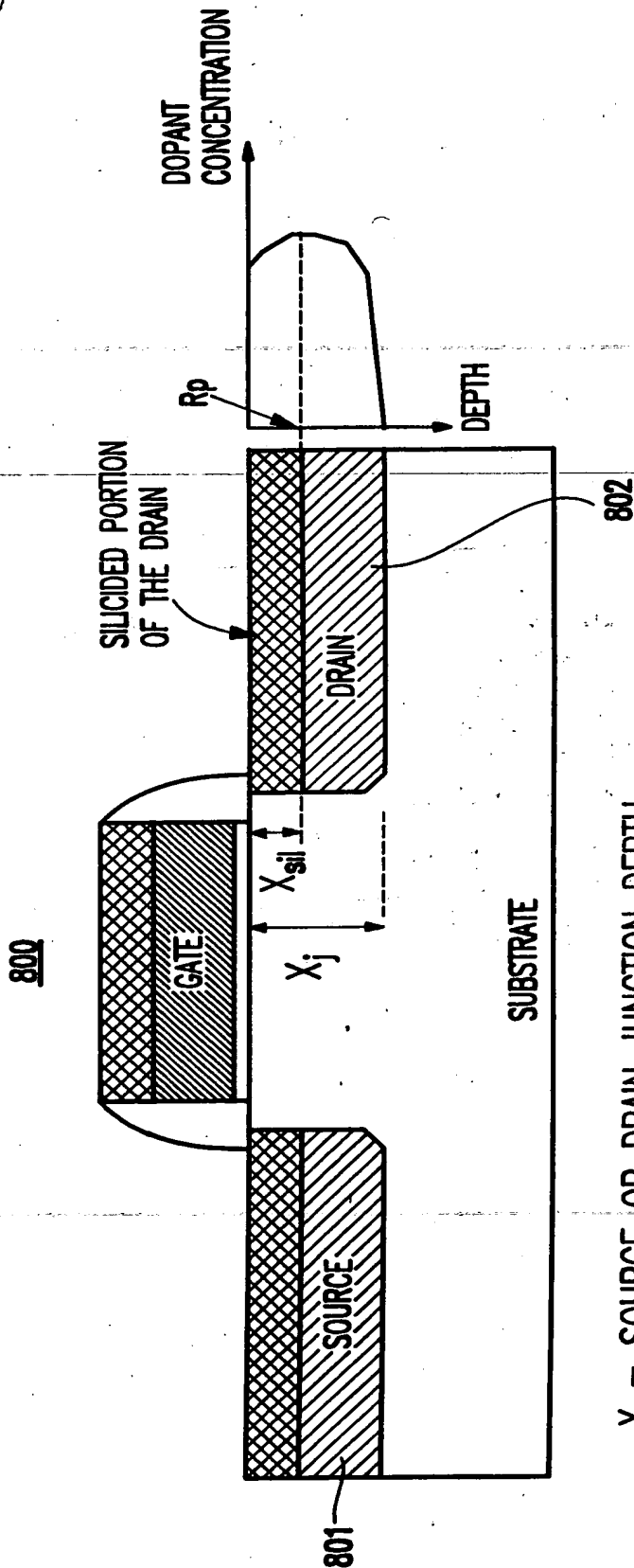


FIG. 7B



X_j = SOURCE OR DRAIN JUNCTION DEPTH

X_{sil} = SILICIDE JUNCTION DEPTH

R_p = PEAK DOPANT CONCENTRATION

REQUIREMENTS:

1. $X_j > X_{sil}$
2. X_{sil} ROUGHLY EQUALS R_p

FIG.8

